PULSE-GENERATOR CIRCUIT AND CIRCUIT ARRANGEMENT

CROSS-REFERENCE TO RELATED APPLICATION

This application is a nation stage of International Patent Application Serial No. PCT/DE2005/000263, filed February 16, 2005, which published in German on September 22, 2005 as WO 2005/088837, and is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

The invention relates to a pulse generator circuit and to a circuit arrangement.

BACKGROUND OF THE INVENTION

Edge-controlled flip flops or edge-controlled master/slave latch pairs are essential basic building blocks for synchronizing multi-stage logic circuits. They are used in almost all modern integrated digital circuits such as digital signal processors (DSPs), microprocessors and integrated circuits for communication applications for increasing the data flow by means of pipelining. For applications with low active power dissipation, flip flops and master/slave latch pairs must still operate reliably and have sufficient switching speed when the difference between a supply voltage V_{DD} and a threshold voltage of the transistors V_T is low, that is to say when the gate overdrive voltage V_{DD}-V_T is low.

In an implementation with modern sub-100 nm or CMOS technologies, it is apparent, however, that the parasitic capacitances of the MOS transistors form a part of the total capacitance to be driven which is not negligible. It is especially the junction and gate overlap capacitances between drain terminal and an internal or external output node which slow down the switching process. Particular attention must be paid to the fact that the gate-drain capacitances appear to be twice as large due to the Miller effect since both the gate potentials and the drain potentials change oppositely on a timescale of approximately 10 ps to 30 ps in the dynamic range.

In contrast to other circuit arrangements such as edge-controlled master/slave latch pairs, edge-